The Metastable Behavior of a Schmitt-Trigger

Andreas Steininger and Jürgen Maier and Robert Najvirt
Vienna University of Technology, 1040 Vienna, Austria
{steininger, jmaier, rnajvirt}@ecs.tuwien.ac.at

***Abstract*—Schmitt-Trigger circuits are the method of choice for converting general signal shapes into clean, well-behaved digital ones. In this context these circuits are often used for metastability handling, as well. However, like any other positive feedback circuit, a Schmitt-Trigger can become metastable itself. Therefore, its own metastable behavior must be well understood; in particular the conditions that may cause its metastability.**

In this paper we will build on existing results from Marino to show that (a) a monotonic input signal can cause late transitions but never leads to a non-digital voltage at the Schmitt-Trigger output, and (b) a non-monotonic input can pin the Schmitt-Trigger output to a constant voltage at any desired (also non-digital) level for an arbitrary duration. In fact, the output can even be driven to any waveform within the dynamic limits of the system. We will base our analysis on a mathematical model of a Schmitt-Trigger's dynamic behavior and perform SPICE simulations to support our theory and confirm its validity for modern CMOS implementations. Furthermore, we will discuss several use cases of a Schmitt-Trigger in the light of our results.

I. Introduction

It is a fundamental task in digital computation to discriminate the analog voltage levels carried by the signal rails in the physical implementation in two logical classes, namely those representing a logic HI and those representing a LO. That can normally be managed by the conventional input stages of logic gates. However, when there is a need for handling less "clean" signals with intermediate voltage levels, slow transitions, or large noise, special provisions are required. This may happen at interfaces or when external disturbances come into play, or in case of metastability of an internal bistable element which can also be caused by clean but badly timed signals. The standard solution for this is the use of a Schmitt-Trigger (S/T) circuit. Unlike a plain discriminator circuit that uses just a single constant reference voltage V_T for separating into HI (above V_T) and LO (below V_T) digital values, the S/T exhibits a hysteresis at its input by switching the reference voltage between V_H and V_L (with $V_H > V_L$) in dependence of its current output state, with V_H being applied when the output is LO and V_L for a HI output[1]. This facilitates stability against noisy input voltages in the proximity of the threshold that typically cause the discriminator to oscillate.

This research was partially supported by the SIC project (grant P26436-N30) of the Austrian Science Fund (FWF).

[1]For the conceptual part of our analysis we consider a non-inverting S/T, while later, in context with the practical design we will study its inverting version that is easier to implement.

Clearly, the original intention of the S/T, namely to discriminate a continuous input voltage space into two subspaces, does not imply a stateful behavior. However, the hysteresis behavior desired for noise immunity does. This caused some uncertainty about whether a S/T can become metastable. Thanks to the results of researchers like Marino [1] and Chaney [2] it is today clear that a S/T, like any other circuit relying on positive feedback, cannot be protected from metastability and will therefore exhibit irregular behavior for some input voltage traces. Still S/Ts are sometimes proposed for filtering metastable outputs of bistable elements [3], or for uniquely classifying the logic level of a node that is intentionally left floating for some time in order to leverage the parasitic capacitance as a dynamic storage element [4], [5]. So one may ask whether such approaches can actually work. In other cases (e.g. [6]), it is hoped that for input voltages with restricted dynamics a S/T will never experience metastability. Again something to check for in more detail.

In this paper we extend existing results – mainly those from Marino [1] – to answer some of these questions that frequently plague designers in practice. To this end we will, after giving a background in Section II, characterize the metastable behavior of the S/T in detail and compare it to that of a typical bistable element (e.g. latch) in Section III. Since metastability is usually a very rare phenomenon that eludes an experimental evaluation, our aim is to give theoretically well founded answers and particularly identify those conditions under which metastability of the S/T can be ruled out for sure. Here we will investigate different scenarios like monotonic and slowly changing inputs. Next, in Section IV we will validate our theoretical results by selected SPICE simulations. In Section V we will investigate concrete use cases of a S/T in the light of our findings. Finally, in Section VI we will conclude our paper.

II. Background

A. Metastability

Metastability is the phenomenon when a bistable element persists in an unstable equilibrium, the metastable state, for a prolonged time. The existence of a metastable state is a fundamental property of every bi- or multistable system – between every two stable equilibria there necessarily is an unstable equilibrium. The difference lies in the behavior when the equilibrium state is slightly disturbed: The system would return to a stable state, however, upon the slightest disturbance from a metastable state, the latter is left in favor of either of the stable states.

It is well understood [7] that every bistable element can be brought to a metastable state in which it may rest for an unbounded time. The manifestation of the metastable state can be oscillation or "creeping" [8]. In the creeping case, which is more relevant here, we know that the classical bistable storage elements (latch, Muller C-element) drive their output at first to a specific "metastable" voltage level V_{meta}, where it stays for an unbounded amount of time, before resolving to one of the stable saturation states. Due to their function V_{meta} must be in between their regular HI and LO states, and, due to symmetry in the design, it is typically an intermediate voltage level in the undefined range V_{xx}. With an appropriately designed threshold of the subsequent stage this creeping behavior can be transformed into a so-called *late transition* where the output of that stage shows a clean transition (i.e. fast crossing of the intermediate levels) but only after metastability has resolved. However, with a single threshold (i.e. without hysteresis) one also introduces the risk of glitches [3].

Metastability is a very undesired phenomenon, as V_{meta} may, beyond the above-mentioned glitches, lead to different ("Byzantine") interpretations by input stages it supplies (as these will most likely have slightly different thresholds), while a late transition can cause timing violations downstream. Unfortunately, in general it can not be avoided completely.

Note that the above applies to bistable storage elements, whose metastable behavior is already well researched – we will have to revisit this for the S/T.

B. Feedback Circuits

The arrangement shown in Fig. 1 represents the fundamental layout of a feedback circuit. A linear voltage amplifier with gain A receives as its input the sum of an external input voltage and its own output voltage multiplied with a factor of k. Its (static) transfer characteristic can be described by

$$G = \frac{V_{out}}{V_{in}} = \frac{-1}{k - \frac{1}{A}} \tag{1}$$

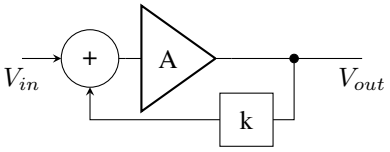
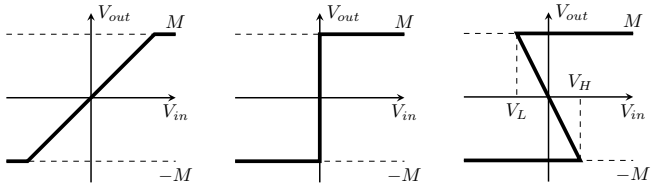


Fig. 1: Basic structure of a feedback circuit

In the case of $k < 0$ we have *negative feedback*. For the moment, let us assume $A = \infty$. Then the arrangement operates as an amplifier with (positive) gain G of $-1/k$. For $k = -1$ we feed back the full output voltage and obtain $G = 1$, i.e. a voltage follower. For $k = 0$ we have no feedback, hence an *open loop*. This arrangement resembles the function of an ideal discriminator whose output assumes the positive saturation voltage M in case $V_{in} > 0$ and changes to the negative saturation[2] $-M$ as soon as $V_{in} < 0$.

[2]For simplicity of explanation we assume symmetric saturation voltages, i.e. +M and -M here. Although the quantitative results will differ in the asymmetric case, our reasoning and our basic conclusions will still hold.

With $k > 0$ we realize *positive feedback*. Now every little change ε on the input produces a change on the output in the same direction that gets fed back and thus further supports the original input change by being added to ε. This self-supporting chain ultimately causes V_{out} to run into positive or negative saturation. In this situation the loop feeds back a voltage of $V_{FB} = Mk$ (or $-Mk$, respectively) that must be compensated in the summation by the input voltage, i.e. $V_{in} < -Mk$ (or $V_{in} > Mk$, respectively) to move the output to the other direction, where it again saturates. This resembles the function of a *Schmitt-Trigger* with hysteresis $V_{hyst} = V_H - V_L = 2Mk$.



(a) $k = -1$ (b) $k = 0$ (c) $k = +\frac{1}{2}$

Fig. 2: Transfer characteristic of a feedback circuit

Fig. 2 shows the characteristics V_{out} over V_{in} for different selections of k. We observe that for negative feedback we have a unique mapping from V_{in} to V_{out}, while for positive feedback V_{out} depends on the current state for $V_L \leq V_{in} \leq V_H$, i.e. we have a hysteresis behavior. Note carefully that the saturation states are the only "truly" stable states of the S/T. The line described by Eq. 1 describes the metastable states only. A very intuitive explanation of this fact is that for a given input voltage $V_L \leq V_{in} \leq V_H$ we can draw a vertical line to find the corresponding steady-state values of V_{out}. This line has three intersections with the characteristic, namely at the positive and negative saturation, as well as one in between. Since we know that the saturation states represent truly stable states, there must be a metastable state in between – irrespective of the implementation. The transient behavior, i.e. the transition from one saturation voltage to the opposite one, depends on the dynamic characteristics of the circuit which are not considered in the basic model in Fig. 1.

For a non-ideal amplifier with $A < \infty$ we obtain a reduction of the effective k by $\frac{1}{A}$ (see Eq 1). In case of negative feedback this reduces the overall gain accordingly, and in case of the S/T it moves the thresholds towards a reduced hysteresis. The borderline case of discriminator operation now occurs for $k = \frac{1}{A}$. Apart from that shift in the value of G (that can be compensated by appropriate dimensioning), all qualitative findings from above, however, remain the same. In Fig. 2 we would, e.g., simply have to replace all instances of k by $k - \frac{1}{A}$. Furthermore, a reference voltage can be added to the feedback path to create a hysteresis that is no more centered around $V_{in} = 0$. Again, while this shift obviously changes the quantitative results, the qualitative findings still hold.

C. Schmitt-Trigger Implementation

A straightforward implementation of the principle from Fig. 1 is by means of an operational amplifier (OpAmp). Since

OpAmps usually have a high gain, this implementation is close to the ideal case of $A \to \infty$.

For negative feedback the feedback path is simply connected to the inverting input, thus effectively realizing the negative sign. For positive feedback the non-inverting input of the OpAmp must be used, which leaves only the inverting input for connecting V_{in}. This means that from the view of the input voltage the function of the S/T circuit is inverting.

In both cases a resistive voltage divider can establish $|k| = \frac{R_B}{R_A+R_B} < 1$, and the feedback path can be augmented with a reference voltage source V_R that will create a horizontal shift of the characteristic. In case of positive feedback this results in a shift of the threshold voltages by an amount of $(1-k)V_R$.

In digital CMOS logic circuits OpAmps are expensive to realize. Therefore a different circuit structure has become common, namely a kind of extended inverter stack with feedback from the output, as shown in Fig. 3.

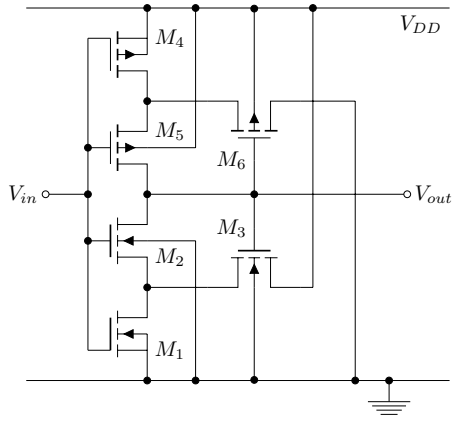


Fig. 3: Conventional CMOS S/T implementation (from [9])

There are different variations to this basic scheme, targeting at low supply voltage [10] or adjustable thresholds [11], [12]. In [9] a detailed mathematical analysis of this circuit is given.

D. Metastability Model for the Schmitt-Trigger

There has been (and sometimes still is) uncertainty whether or under which circumstances a S/T is prone to metastability, as its function of classifying an input voltage (rather than storing data) appears combinational. However, as Fig. 2 and the associated explanation in Sec. II-A show, *every* positive feedback circuit *must* have a metastable state. Note, that this curve resembles a general model of a positive feedback circuit without being limited to a specific implementation.

Fig. 4 shows how an RS-latch can be constructed from a S/T. This gives an intuition that the latter must have storage capabilities. It also indicates that building a perfect S/T is equivalent to building a perfect RS-latch, which we know is impossible [7].

There has also been quite some debate on whether a S/T can be applied to construct a synchronizer flip flop that is immune against metastability (e.g. [13], [2]). This discussion has been resolved in a paper by Marino [1] in which he proposes a dynamic model for the S/T circuit as follows: He augments

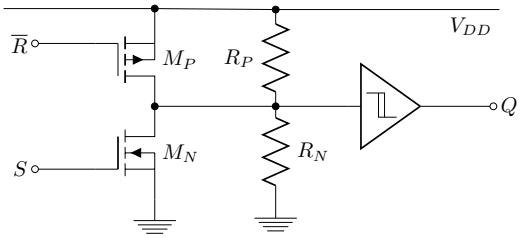


Fig. 4: RS-latch implementation based on a S/T

the OpAmp realization with a low-pass (R_0C_0) at the output to account for its dominant time constant, and thus approximates the dynamic behavior in the model. He assumes another RC element at the inverting input and a reference voltage V_R to obtain thresholds that are not bound to be symmetric around 0. A simplification of his model circuit used in this paper is shown in Fig. 5. To be more general, we will, compared to Marino's circuit, drop the input RC element, and we use more intuitive names (V_{in} for V_2 and V_{out} for V_q).

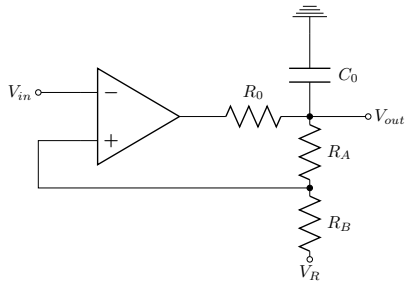


Fig. 5: Dynamic model of the S/T inspired by Marino [1]

As the saturation requires separate treatment, his solution comprises three regions, namely upper and lower saturation (Regions 1 and 3), as well as the "linear region" 2 between them. Fig. 6 illustrates his solution. Note that, according to the implementation of the model circuit, this diagram applies to an inverting S/T.

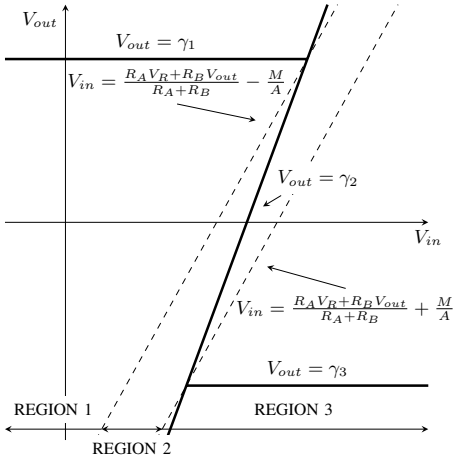


Fig. 6: Phase diagram for the S/T inspired by Marino [1]

The dashed lines in the figure represent the borders between the regions (the corresponding equations are shown as well).

They are derived by determining those values for the OpAmp's differential input voltage for which it starts to saturate. Ultimately, Marino obtains the following equations (for their detailed derivation please refer to the original paper):

$$\text{Region 1:} \qquad \frac{dV_{out}}{dt} = V'_{out} = -\frac{1}{\tau_1}(V_{out} - \gamma_1) \qquad (2)$$

This yields a decaying exponential function with time constant $\tau_1 \approx R_0 C_0$ that asymptotically approaches the truly stable rest point $\gamma_1 \approx M$.

$$\text{Region 2:} \qquad \frac{dV_{out}}{dt} = V'_{out} = \frac{1}{\tau_2}(V_{out} - \gamma_2) \qquad (3)$$

This time we have a growing exponential function with time constant $\tau_2 \approx \frac{R_0 C_0}{kA-1}$ that moves away from the metastable rest point $\gamma_2 \approx \frac{V_{in}-(1-k)V_R}{k-\frac{1}{A}}$. Note that this rest point now depends on the input voltage.

$$\text{Region 3:} \qquad \frac{dV_{out}}{dt} = V'_{out} = -\frac{1}{\tau_3}(V_{out} - \gamma_3) \qquad (4)$$

Similar to Region 1 this yields a decaying exponential function with time constant $\tau_3 = \tau_1 \approx R_0 C_0$ that asymptotically approaches the truly stable rest point $\gamma_3 = -\gamma_1 \approx -M$.

Marino uses this model to show that a S/T can neither be used to build a perfect inertial delay element nor a perfect synchronizer. Although his model clearly shows that a S/T may indeed become metastable, in his argumentation he is mainly concerned with the question of whether it can be driven to produce runt pulses or glitches at its output. He shows that this is indeed possible, even if restrictions for the input are applied. He does, however, not consider other metastability effects like transition delay or constant output voltage and under which circumstances these occur. Similarly, Nyström and Martin [4] as well as Greenstreet [5] limit their discussions to the special case of monotonic input voltage only.

In this paper we build on Marino's model, but extend the scope towards typical use cases, validate the model for a modern CMOS implementation, provide a more general treatment of the metastable behavior of a S/T, and give a deeper analysis of the case of monotonic input voltage than in [4], [5].

III. Analysis of Metastable Behavior

A. Peculiarities in the Schmitt-Trigger's metastable behavior

Fig. 6 suggests that a S/T can assume different metastable points V_{meta}; in fact along the whole line γ_2. This is substantially different from what is known for typical bistable storage elements, whose (internal storage cell's) metastable output voltage is confined to a single value in the V_{xx} range. The metastable behavior of a latch cell has been first modeled by Veendrick [14], and his analysis forms the theoretical foundation of what we know about metastable behavior of bistable storage elements today. So let us compare Marino's model with that used by Veendrick to spot the differences. In both models a linear amplifier is employed, and its dynamic behavior is approximated by a first order low pass. So not surprisingly the solutions are exponential functions in both cases and hence similar. However there are two important differences:

1) For his latch circuit Veendrick assumes the input to be decoupled (opaque state) and just studies the homogeneous behavior, while Marino, for his S/T model needs to leave the input voltage connected all the time. As a result, Marino's solution shows a dependence of the metastable rest point on the input voltage in Region 2, rather than just a single metastable point.
2) As a consequence of (1), Veendrick could concentrate his analysis on the proximity of the metastable point, while Marino had to consider the whole operating range and therefore needed the case separation.

So (1) gives us an intuitive confirmation why the S/T has a whole range of metastable points. Conceptually, this appears to be due to the fact that, having only one input, the S/T derives its trigger for the state change from the amplitude of this single signal, making a constant observation necessary, while all bistable storage elements have two inputs and can hence decouple either of them temporarily.

B. Regular operation

We will base most of our reasoning on the phase diagram (Fig. 6). So let us first observe the normal operation of the S/T there: We start in the positive saturation in Region 1 (for the rest of the paper we will always consider the positive saturation as a starting point, while due to symmetry, equivalent arguments can be given for starting in the negative saturation) As we increase V_{in} we move along γ_1 until we reach V_H. Up to this point we have no freedom in choosing the trajectory, and the shape of V_{in} is irrelevant. Only after crossing V_H the S/T will leave the stable state and start moving towards the negative saturation. During this phase – and only then – we have the opportunity to manipulate the trajectory and force the S/T back to the initial state, or maneuver it into a metastable state. Here the shape of V_{in} matters a lot. We will investigate more details on that later. Once in the negative saturation, the same procedure starts over in the other direction.

C. Monotonic input

Let us again start on some point along γ_1. Exceeding V_H then implies a positive slope of V_{in}, and all trajectories reachable with a monotonic V_{in} are hence within the half plane $V_{in} > V_H$ where there is no metastable point (recall that the latter are all located on γ_2). In fact V_{in} need not even be monotonic, as long as it does not fall back to below V_H.

Fig. 7 shows the first derivative dV_{out}/dt over the phase diagram according to Eq. 2 to 4. We have chosen $A = 10$ for this plot, which is way too low for a typical OpAmp, but for higher values Region 2 would be hard to recognize (its width is just $\frac{2M}{A}$). V'_{out} represents the speed at which the trajectory is pulled upward ($V'_{out} > 0$) or downward ($V'_{out} < 0$) by the internal dynamics of the circuit. We observe that if, starting

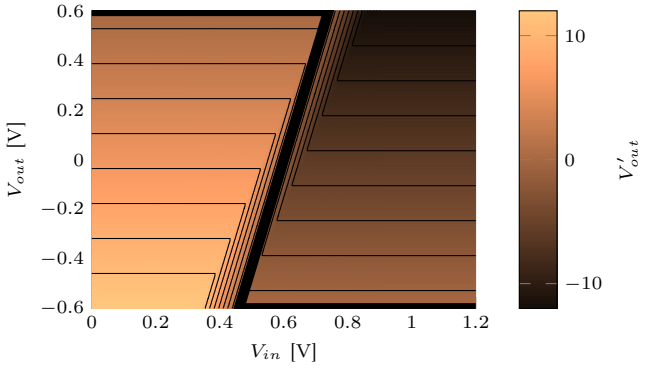


Fig. 7: Derivative of the output voltage over the phase diagram

from positive saturation, we apply a step function to move to an operating point very close to but above the threshold, say $(V_{in}, V_{out}) = (V_H + \varepsilon, \gamma_1)$ the downward speed V'_{out} is close to zero, so V_{out} will initially change very slowly. This suggests we obtain a slow output transition. To determine the duration of this transition, let us first assume our step input takes us right into Region 3, i.e. $\varepsilon > \frac{2M}{A}$. Then for constant $V_{in} = V_H + \varepsilon$, Eq. 4 predicts a decaying exponential function from γ_1 towards γ_3 according to

$$V_{out}(t) = (\gamma_1 - \gamma_3) \cdot e^{\frac{-t}{\tau_3}} + \gamma_3 \tag{5}$$

Now we assume a threshold V_{th} for the subsequent stage to recognize V_{out} as being LO with $V_{th} = \gamma_3 + \sigma \cdot (\gamma_1 - \gamma_3)$, with $0 < \sigma < 1$ giving the proportion of the swing that V_{th} is apart from the final value (that is reached asymptotically). This value will be reached with a delay of

$$D_{III} = \tau_3 \cdot ln\left(\frac{1}{\sigma}\right) \tag{6}$$

after having applied the input step. Note that, as long as we remain within Region 3, this value is independent of V_{in} (and hence ε) and therefore stays the same, even if we apply larger steps. It is the minimum switching time of the S/T.

For $\varepsilon \in [0, \frac{2M}{A}]$ we start the trajectory in Region 2. Again with constant V_{in} it will move downward and cross the boundary to Region 3 at some point. Up to that point V_{out} will follow a growing exponential function according to

$$V_{out}(t) = -\frac{\varepsilon + \frac{\gamma_1 - M}{A}}{k - \frac{1}{A}} \cdot e^{\frac{t}{\tau_2}} + \frac{\gamma_1 k - \frac{M}{A} + \varepsilon}{k - \frac{1}{A}} \tag{7}$$

and the time needed for the trajectory to move through Region 2 becomes approximately

$$D_{II} = \tau_2 \cdot ln\left(\frac{2M}{A\varepsilon}\right). \tag{8}$$

At the region boundary the decaying function from Eq. 5 will take over. Fig. 8 shows a simulation result (for details on the setup see Section IV) that illustrates the situation.

The transition time is the sum of $D = D_{II} + D_{III}$ (with a small error due to D_{III} actually being valid for the full swing).

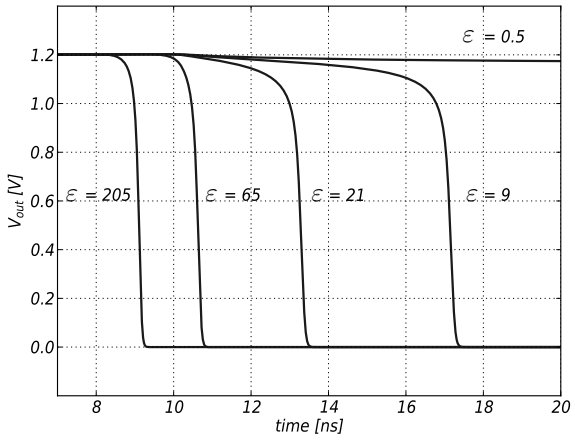


Fig. 8: Falling output transitions for different ε in mV

The simulation results for the CMOS implementation shown in Fig. 8 confirm that the simplified OpAmp model does a good job in predicting the behavior. In particular one can verify that D_{II} dominates, especially for small ε. It is interesting to note that using Veendrick's model [14] for calculating the required resolution time D_{meta} of a latch from a metastable state yields, similar to our result, a D_{meta} proportional to the metastability time constant τ_C and to $ln(\frac{1}{V_\Delta})$ with V_Δ being the initial voltage disparity.

The γ_n lines are by definition the only places where V'_{out} becomes zero. So, due to the continuity of V'_{out} proven in [1], the sign of V'_{out} stays the same as long as we do not cross a γ_n line. This can also be verified in Fig. 7. As a consequence we have a strictly decreasing V_{out} in the above cases of $\varepsilon > 0$, even if the start may be arbitrarily slow. Although this can be regarded as what is normally called a late transition in the context of bistable elements, we have a fundamentally different metastable behavior in the S/T: This late transition is due to resolution of a metastable state that is associated with a clean HI level. In contrast, for bistable storage elements the metastable state is necessarily associated with resting at an intermediate voltage in the range V_{xx} between the element's clean HI and LO outputs, and the late transition is a secondary effect caused by applying a high or low threshold [3].

D. Producing a constant output voltage

Let us now study the possibility of driving the S/T into an arbitrary metastable state: Assume we start again on γ_1. Once V_{in} exceeds V_H our operating point is right of γ_2, and the internal dynamics of the S/T is moving us downward ($V'_{out} < 0$). In order to reach a metastable operating point on γ_2 we need to reduce V_{in} fast enough to make the trajectory intersect with γ_2 before the negative saturation is reached. Due to the inclination of γ_2 the amount by which we have to reduce V_{in} grows as V_{out} moves downward. In addition, $V'_{out} < 0$ becomes larger with the operating point's distance from γ_2. So once that distance is large, it takes a highly dynamic change in V_{in} to reach a metastable point. Contrariwise, when staying close to γ_2 right from the start, V'_{out} can be kept as

small as desired, leaving enough time for an arbitrarily slow change in V_{in} to reach a metastable point on γ_2 at any desired intersection point.

As can be seen in Fig. 6, γ_2 provides a one-to-one mapping between V_{in} and V_{out}. So with an appropriate choice of the final value of V_{in} (i.e. once having the threshold crossings accomplished), any value of V_{out} can be selected. Notice that this property allows us to freely select the metastable output voltage of the S/T based latch sketched in Fig. 4 by proper adjustment of the voltage divider.

E. Creating an arbitrary output shape

In principle, by appropriately navigating in the phase diagram one can obtain any desired shape of V_{out}: For every current value of V_{out} an appropriate V_{in} can be applied to obtain the desired gradient V'_{out} (by crossing γ_2 even the sign can be changed). However, with a limited range of V_{in} only a limited range of V'_{out} can be covered (see Fig. 7); in other words, the dynamics of V_{out} is naturally limited by the system dynamics. The second limitation is the dynamics of V_{in}. Assume an operating point with a horizontal distance X and vertical distance of $Y = \alpha \cdot X$ from γ_2, with $\alpha \approx \frac{1}{k-\frac{1}{A}}$ being the slope of the latter. According to Eq. 3 V'_{out} has a value of $\frac{Y}{\tau_2}$ at this point. Moving the trajectory closer towards γ_2 takes a V'_{in} larger (in absolute value) than $\frac{V'_{out}}{\alpha}$. So for a given maximum gradient $\hat{V}'_{in}$, we obtain a maximum allowed horizontal distance from γ_2 of $|X| < \tau_2 \cdot |\hat{V}'_{in}|$. Once the operating point leaves this corridor around γ_2, there is no way of preventing the trajectory from approaching the saturation of V_{out} in a monotonic trace (For a more elaborate and formal treatment see [1]).

IV. Evaluation

A. Setup and characteristic

To validate our analyses we implemented S/Ts based on an ideal OpAmp, which matched the theoretical model perfectly, a commercial OpAmp (Type EL5165), which showed only minor deviations, and the CMOS circuit from Fig. 3 in HSPICE. As the latter is substantially different from Fig. 5 we wanted to investigate whether Marino's model sufficiently covers its behavior. It was implemented using transistor parameters of a standard inverter cell from an industrial 65 nm technology library, whereat despite a 2 fF output load no interconnect parasitics were considered. The resulting input-to-output characteristic is shown in Fig. 9. It matches the theoretical model (Fig. 6) well, however γ_2 turns out to be not straight but shows an increased slope at the ends. It was determined point by point, in each case starting a transient analysis with a preset pair of $\mathring{V}_{out}$ and $\tilde{V}_{in}$. By sweeping the value of $\tilde{V}_{in}$ we determined the matching $\mathring{V}_{in}$ for which the transient analysis showed stable behavior. The dots in the figure represent V'_{out}, with gray dots for positive values and black dots for negative ones, and with large dot size indicating a large value. The large "corridor" around γ_2 points to a wide Region 2 and hence a low gain A. In addition, we observe a dependence of V'_{out} on γ_2 in the upper right and lower left corner that is not present in the ideal model in Fig. 7. The qualitative results from Section III, however, only require V'_{out} to be consistently positive (negative) on the left (right) side of γ_2 and continuous, so they still hold.

We also analyzed the CMOS circuit using transistor equations to derive an analytical expression for γ_2 (dashed line in Fig. 6). By searching for equilibrium states, i.e. where a constant input leads to a constant output voltage, an explicit formula $V_{out}(V_{in})$ could be derived, assuming transistors M_1 and M_4 operate in their linear region and all others in the saturation one. Unfortunately this assumption is only valid in the middle of the metastable region; at the edges the transistors M_2 and M_3 respectively M_5 and M_6 start to enter their linear operation region. For that reason the analytic expression, while matching with Marino's OpAmp model, does not fit well to the real curve near V_H and V_L.

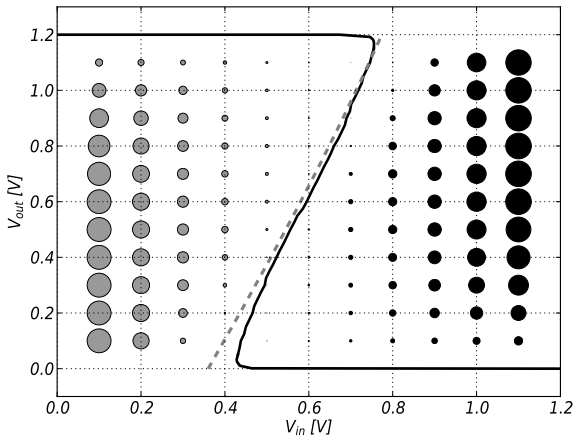


Fig. 9: Derivative of the output voltage over the phase diagram

B. Evaluation of the scenarios from Section III

Our claim was that monotonic input signals will always lead to strictly monotonic outputs. In the simulation shown in Fig. 10 we verified the worst case by applying a ramp input stopping at a constant input voltage close to V_H, i.e. $V_H + \varepsilon$ (dark lines). One can clearly see that in both cases the output transitions are very steep (all with about the same transition time) but, as theory predicts, their delay varies significantly even for small changes in ε.

Fig. 11 illustrates the observed dependence of the output delay on ε in a more global scope. This nicely confirms Eq. 8.

Fig. 12 shows that it is indeed possible to force the S/T to output arbitrary waveforms by means of non-monotonic inputs. In the first part, the figure shows regular operation to demonstrate the dynamics of the S/T as well as its thresholds. Starting at 20 ns, the S/T is driven to output a 100 MHz sine with 0.5 V swing. Note that this requires keeping the S/T metastable. Finally, the simulated S/T is driven into deep metastablity with the input being constant from 58 ns simulation time. Here, the results of two simulations can be seen. In the first, metastability resolves to V_{DD}, in the second, it resolves to *GND*.

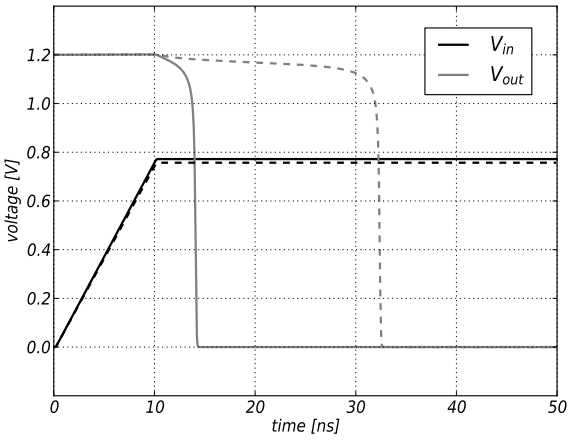


Fig. 10: Late transitions caused by ramp input going slightly above V_H

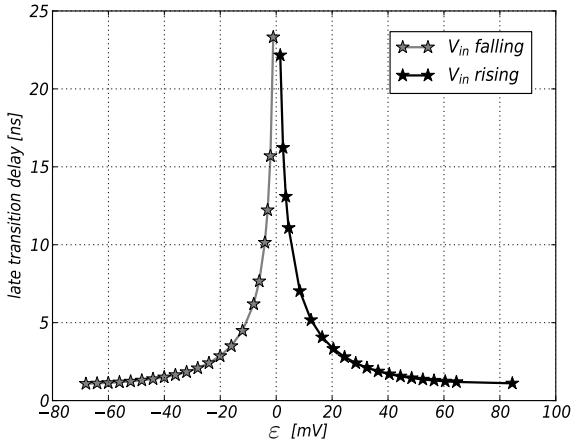


Fig. 11: Observed dependence of output delay on ε

In the phase plot, it can be seen that the generation of the slow (w.r.t. its regular switching speed) sine required to keep the output close to the γ_2 line. The resolution of the metastable state can also be seen as vertical line segments at $V_{in} \approx 0.6\,V$.

This verifies the predictions from Sections III-D and III-E. A constant output voltage can either be generated as an arbitrary waveform by actively controlling the input, or by forcing the S/T into perfect metastability. As before, small changes at V_{in} lead to huge variations in the time progress of V_{out}. The two output traces shown in the figure correspond to input traces only deviating in their final stable voltage by less than $0.1\,\mu$V (not distinguishable in the figure). Clearly, if the appropriate voltage is set with a sufficient precision, it can take an arbitrary time for the metastability to resolve.

Nevertheless, in these simulations we experienced that it takes an *extremely* precise control of the voltage (nV) in order to get close enough to γ_2 such that slow inputs still create visible metastability effects, as theory would predict.

V. Practical Use Cases

A. Handling of intermediate voltages

Often a S/T is applied as a means for converting the intermediate voltage V_{meta} produced by a metastable binary storage element into a clean HI or LO, like e.g. in [3]. As we have seen in our analysis in Section III-C this will actually work under two important conditions:

(1) The input of the S/T must indeed be monotonic, at least in the proximity of the thresholds. This can be easily accomplished in a typical setting, where the (single!) intermediate output voltage V_{meta} is near the middle of the supply range. With thresholds chosen in appropriate distance from V_{meta} one can ensure that these are crossed only when metastability is already resolving, i.e. with an increasing exponential function that is strictly monotonic (for details see [14], [15]). However, care must be taken that it is indeed the S/T that decides upon the classification of V_{meta}. As soon as any other stage (decoupling buffer, e.g.) is in between the metastability-producing element and the S/T, that element's (single!) input threshold will typically classify V_{meta} in an undesired way. More specifically, glitches can be produced [3], with the S/T having no chance to mitigate these.

(2) A delay introduced by the S/T must be accommodated in the timing of the subsequent logic. With properly selected thresholds as outlined above we can assume steep input transitions, so the S/T will not by itself introduce the arbitrary resolution delay discussed in Section III-C. Still it may take an unbounded time until the metastability of the bistable storage element resolves, during which the S/T observes a constant V_{meta} at its input. As its threshold is crossed only after that, the S/T appears to produce a late transition. This is actually an intended behavior, useful for handling metastability in a value safe system, like a speed-independent design [3].

Essentially, (2) is the reason why Chaney [2] and Kleeman et al. [15] correctly state that the use of S/Ts is not beneficial for avoiding metastability in a synchronizer and even degrades the performance. Marino [1], on the other hand, was concerned with inputs not limited to monotonic slope. Therefore his conclusion was, similarly, that the S/T is not useful in avoiding metastability. As we have laid out, however, for the special application of filtering of intermediate voltages from a metastable bistable storage element in value safe environments, the S/T can be safely applied without any residual risk of metastability.

B. Slow inputs

It is sometimes hoped [6] that limiting the dynamics of the input signal can prevent the S/T from getting metastable. The intuition is that the S/T will have accomplished its state change before a (slow) change in the input voltage has had a chance to move the trajectory towards a metastable point. Our analysis in Section III-E has re-confirmed Marino's result that one can always find a corridor around γ_2 small enough to allow an appropriately controlled V_{in} to still reach a metastable point, no matter how restricted its dynamics ($\hat{V}'_{in}$) may be. However, as our simulation experiments showed, it takes an extremely precise control of V_{in} to remain in a sufficiently narrow corridor. So while limiting V'_{in} cannot safely rule out metastability of the S/T, it *does* aid in making metastability less probable.

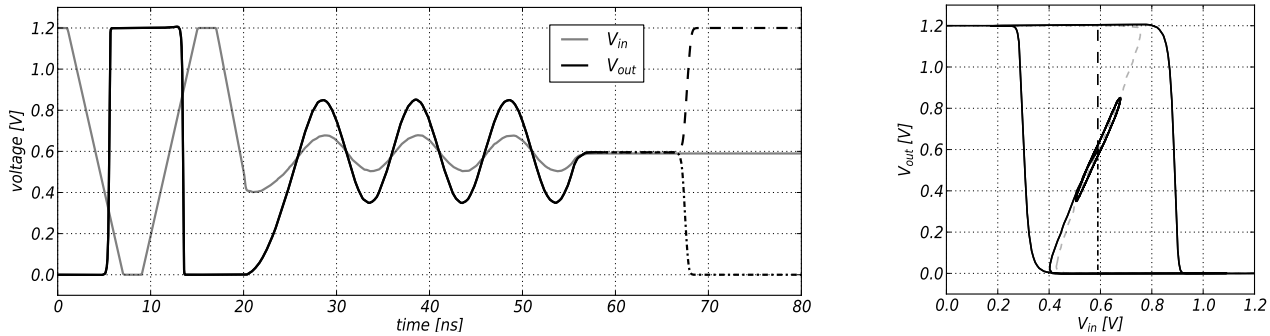


Fig. 12: Simulation trace and phase diagram of an S/T driven to produce regular transitions, an arbitrary (here sine) waveform and to enter and resolve deep metastability

C. Handling slow monotonic inputs

We have given evidence in Section III-C that a S/T can map arbitrarily slow monotonic inputs to steep, practically full-swing transitions. However, metastability can still occur and cause a seemingy sporadic transition during a period with an unchanging input voltage.

One example of such an application is the S/T D-latch implementation from [5], where the application requires handling glitches on the enable input. The input stack is a tri-state inverter that propagates the data input when the latch enable is high, and has a floating output (assumed constant) else. The resulting monotonic signal is fed into a S/T. The author correctly recognizes that even in presence of glitches on the enable input, the S/T would always correctly output steep transitions, albeit with an arbitrary delay.

Another example is the integrator used in the synchronizer and clock to handshake circuits in [4]. Here a precharged high signal is driven low (or vice versa) depending on the state of an external, unstable input. It is also correctly argued that a S/T converts these monotonic inputs to steep transitions, however, the possibility that a signal driven slightly beyond the S/T's threshold and left at that constant voltage may cause arbitrarily delayed output transitions, is not further pursued. The subsequent circuits, being delay insensitive, can tolerate such delayed transitions, however one should be aware of the possibility for such timing variations.

VI. Conclusion

We have revisited existing results on S/T metastability, most notably those from Marino [1], and extended them to elaborate a general understanding of this effect and give well founded answers to a couple of practical questions. In this sense our key contributions are to clearly pinpoint the differences between S/T metastability and that of bistable storage elements, to provide simulation results from a realistic CMOS implementation that back up theoretical results (shape of characteristic, V'_{out} over the phase diagram), to elaborate and validate a function for the output delay, to give solid evidence for the appropriateness of using a S/T for metastability filtering in the value domain, and to elaborate on the benefits of limiting the dynamic range of V_{in}.

Limitations lie in idealizations made in the process of modeling, like the first-order approach for the dynamic behavior, ignoring parasitics, noise and the curved shape of the γ_2 line. In our simulations we have found confirmation that the errors thus introduced are acceptable and therefore the key effects are well reflected in the model, but more details should be explored here, especially for new technologies.

References

[1] L. R. Marino, "The Effect of Asynchronous Inputs on Sequential Network Reliability," *IEEE Transactions on Computers*, vol. 26, no. 11, pp. 1082–1090, 1977.

[2] T. Chaney, "Comments on "A Note on Synchronizer or Interlock Maloperation"," *IEEE Transactions on Computers*, vol. C-28, no. 10, pp. 802–804, Oct 1979.

[3] T. Polzer and A. Steininger, "SET propagation in micropipelines," in *Power and Timing Modeling, Optimization and Simulation (PATMOS), 2013 23rd International Workshop on*, Sept 2013, pp. 126–133.

[4] M. Nyström and A. Martin, "Crossing the synchronous-asynchronous divide," in *Workshop on Complexity-Effective Design*, Anchorage, AK, May 2002.

[5] M. Greenstreet, "Real-time merging," in *Fifth International Symposium on Advanced Research in Asynchronous Circuits and Systems*, 1999, pp. 186–198.

[6] (2015/11/22) http://electronics.stackexchange.com/questions/174079/do-schmitt-trigger-specs-give-requirements-to-avoid-metastability.

[7] L. R. Marino, "General Theory of Metastable Operation," *IEEE Transactions on Computers*, vol. C-30, no. 2, pp. 107–115, Feb. 1981.

[8] T. Kacprzak, "Analysis of oscillatory metastable operation of an RS flip-flop," *IEEE Journal of Solid-State Circuits*, vol. 23, no. 1, pp. 260–266, Feb 1988.

[9] I. Filanovsky and H. Baltes, "CMOS Schmitt trigger design," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 41, no. 1, pp. 46–49, Jan 1994.

[10] P. Singhanath, A. Suadet, A. Kanjanop, T. Thongleam, S. Kuankid, and V. Kasemsuwan, "Low voltage adjustable CMOS Schmitt trigger," in *2011 4th International Conference on Modeling, Simulation and Applied Optimization (ICMSAO)*, April 2011.

[11] Z. Wang, "CMOS adjustable Schmitt triggers," *IEEE Transactions on Instrumentation and Measurement*, vol. 40, no. 3, pp. 601–605, Jun 1991.

[12] V. Katyal, R. Geiger, and D. Chen, "Adjustable hysteresis CMOS Schmitt triggers," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2008, pp. 1938–1941.

[13] E. Wormald, "A Note on Synchronizer or Interlock Maloperation," *IEEE Transactions on Computers*, vol. C-26, no. 3, pp. 317–318, March 1977.

[14] H. J. Veendrick, "The behaviour of flip-flops used as synchronizers and prediction of their failure rate," *IEEE Journal of Solid-State Circuits*, vol. 15, no. 2, pp. 169–176, Apr 1980.

[15] L. Kleeman and A. Cantoni, "Metastable Behavior in Digital Systems," *IEEE Design Test of Computers*, vol. 4, no. 6, pp. 4–19, Dec 1987.